Matching transistors **120** and **122** form the $\Delta V_{be}/R$. The area ratio is 9:1 and the current ratio, determined by MOSFETs **126** and **128**, is 1:5 so that

$$\Delta Vbe = V_t \ln 45,\ V_t = \frac{kt}{9},\ 45 = 9xs$$

$$\Delta Vbe \sim 100mv$$

$$I_{ref} = \frac{\Delta Vbe}{R} = \frac{0.1}{R}A = \frac{100}{R(k\pi)}\mu A$$

MOSFETs **130**,**132**,**133**, and **136** form the amplifier. The output of the amplifier V_{out} is the drains of MOSFETs **130** and **136**. The configuration is such that $\Delta V_{be}/R$ is mirrored from the source of MOSFET **132** to analog ground.

Other devices in circuit **35** are provided for startup, stability and to increase power supply rejection ratio. Preferably, in order to approach an ideal result, certain groups of devices are matched: Transistors **120** and **122**; MOSFETs **130** and **132**; MOSFETs **126**, **128**, and **138**; MOSFETs **134**, **136**, and **140**. Accordingly, ΔV_{be} depends only on the above matching and temperature.

$$\Delta V_{be} = \frac{kt}{9} \ln \text{ (area ratio} \times \text{current ratio)}.$$

I_{ref} will then only depend on absolute value of R, as follows:

$$Iref = \frac{\Delta Vbe(T)}{R(T)}$$

If R(T) tracks ΔV_{be} (T) with respect to temperature, then I_{ref} will be independent of temperature, and will depend only on absolute value of R. Using P_{body} and SP+ to get the correct temperature on R, R can be made to ±10% accuracy, so I_{ref} will have ±10% accuracy (assuming matching and n factor ideal).

A plurality of current reference signals can be provided to various portions of the IC by way of block **150**.

Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. Therefore, the present invention is limited not by the specific disclosure herein, but only by the appended claims.

What is claimed is:

1. A current sense integrated circuit, comprising:

an amplifier circuit for receiving and amplifying a differential analog input signal at a first voltage level containing current sense information, wherein the amplifier circuit includes a circuit to minimize inherent temperature offset drift;

a pulse width modulator circuit for converting the differential analog input signal to a pulse width modulated signal at the first voltage level;

a level shift circuit for converting the pulse width modulated signal from the first voltage level to a second voltage level; and

a recovery circuit for reconstructing the analog input signal at the second voltage level.

2. The current sense integrated circuit of claim **1**, wherein the circuit to minimize inherent temperature offset drift comprises a pair of mirrored MOSFETs, such that the circuit has an offset voltage which is equal to the difference between the gate-to-source voltage of the MOSFETs and remains constant over temperature variations.

3. The current sense integrated circuit of claim **1**, wherein the level shift circuit comprises a pulse generator circuit for producing rising edge triggered pulses and falling edge triggered pulses from the pulse width modulated signal and a pair of MOSFETs for receiving the rising edge triggered pulses and the falling edge triggered pulses and transposing those pulses from the first voltage level to the second voltage level.

4. The current sense integrated circuit of claim **1**, further comprising a high side current reference circuit.

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